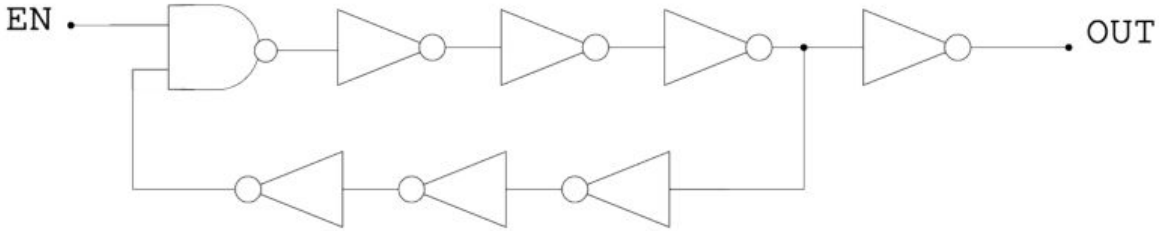
Ring oscillator

10 MHz Ring Oscillator Design Project



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Specifications



Edu4Chip full custom design track - Jean Max

- Ring oscillator with a target frequency of 10MHz ±5%
- As small layout as possible

Theory - Frequency of a ring oscillator

$$f = \frac{1}{2 \cdot N \cdot t_{pd}}$$

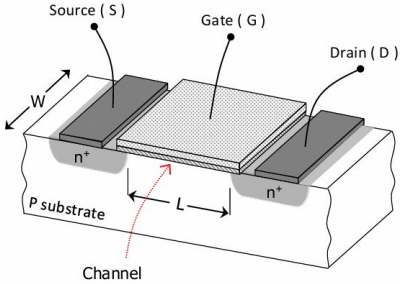
$$R \propto \frac{L}{W}, \quad C \propto W \cdot L, \quad t_{pd} \propto R \cdot C = L^2$$

$$f \propto \frac{1}{t_{pd}} \Rightarrow f \propto \frac{1}{L^2}$$

The frequency is proportional to the inverse of the length squared!

Parameters

- f - Frequency
- N - Number of inverters
- t_{pd} - Propagation delay
- R - Resistance
- C - Capacitance
- W - width
- L - length



Edu4Chip intro-day slides - Jean-Max

Initial inverter schematics simulations

Parameters

t_{pd} = 20ps

L = 180nm

W_{nmos} = 1µm



Theory - Length of the inverter

$$f = \frac{1}{2 \cdot N \cdot t_{pd}}$$

$$f_{goal} = \frac{1}{2 \cdot N \cdot t_{pd-o} \cdot \left(\frac{L_n}{L_o}\right)^2}$$

Isolating for L_n

$$L_n = \frac{\sqrt{2}\, L_0}{2\sqrt{f \cdot N \cdot t_{pd-o}}} \approx \boxed{2{,}7\mu m}$$

New inverter length

Known parameters

f_{target} - 10MHz
N - 11
t_{pd-o} - 20ps
L_o - 180nm

NAND

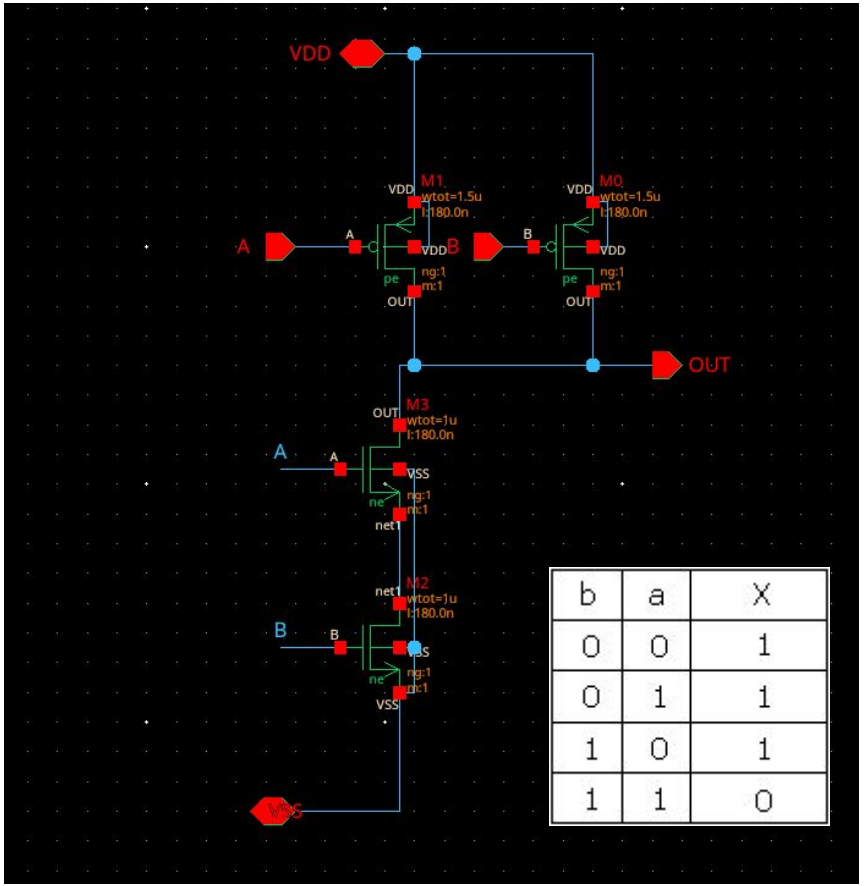
- Output goes low => A·B = 1

  → A **AND** B high. NMOS conduct on a high gate, and "AND" means both must conduct → **series**.

- Output goes high when X = 1 = (A·B)′ = A′ + B′, i.e.

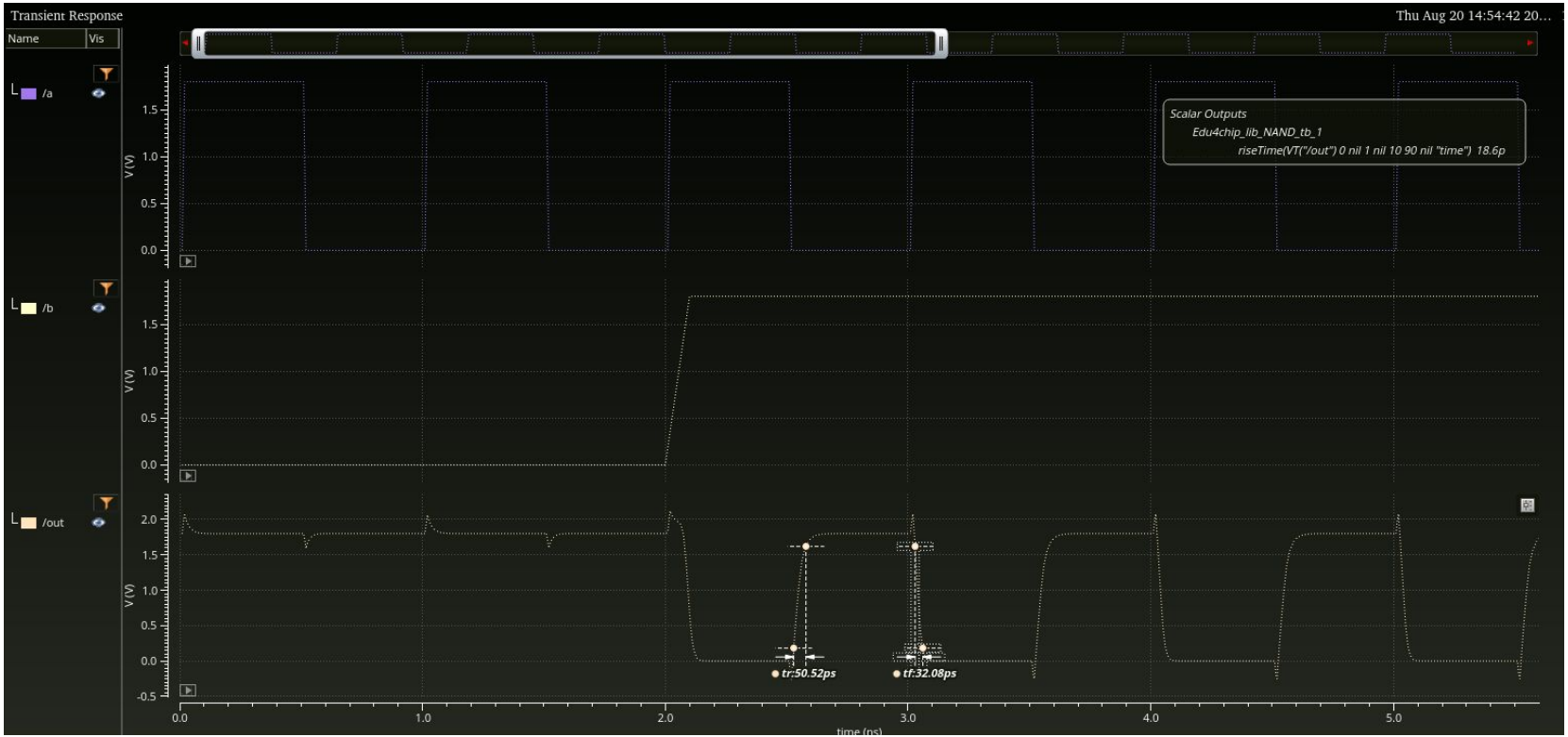
  →A **OR** B low. PMOS conduct on a low gate, and "OR" means either one suffices

  → **parallel**.



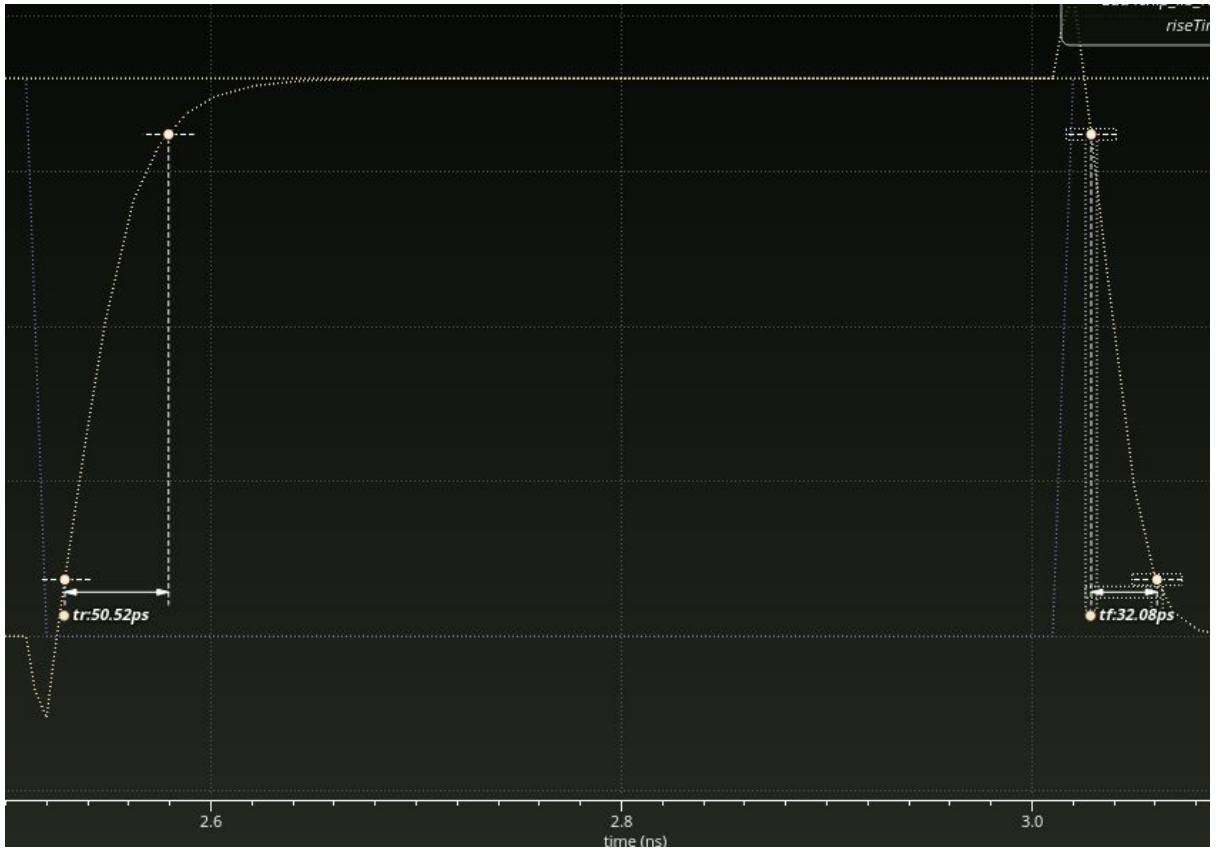
b	a	X
0	0	1
0	1	1
1	0	1
1	1	0

NAND


Transient Response
Thu Aug 20 14:54:42 20...
Name
Vis
/a
/b
/out
V (V)
Scalar Outputs
Edu4chip_lib_NAND_tb_1
riseTime(VT("/out") 0 nil 1 nil 10 90 nil "time") 18.6p
tr:50.52ps
tf:32.08ps
time (ns)

NAND

rise and fall time measurements

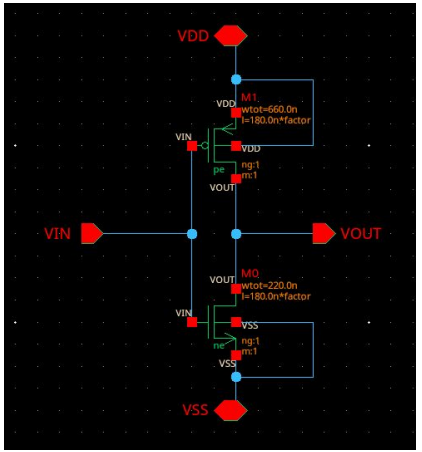


Inverter

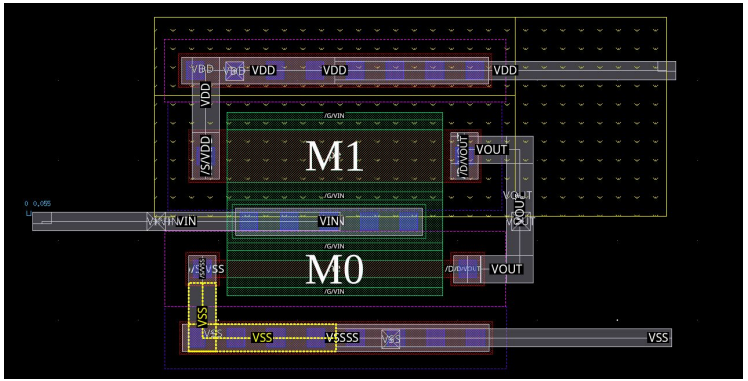
(propagation delay)

- Schematic:
  - based on full custom lab design
  - adjustment of parameters
- Layout:
  - extended power and ground rails for efficient inverter chaining
  - extended input wire for immediate connection to output

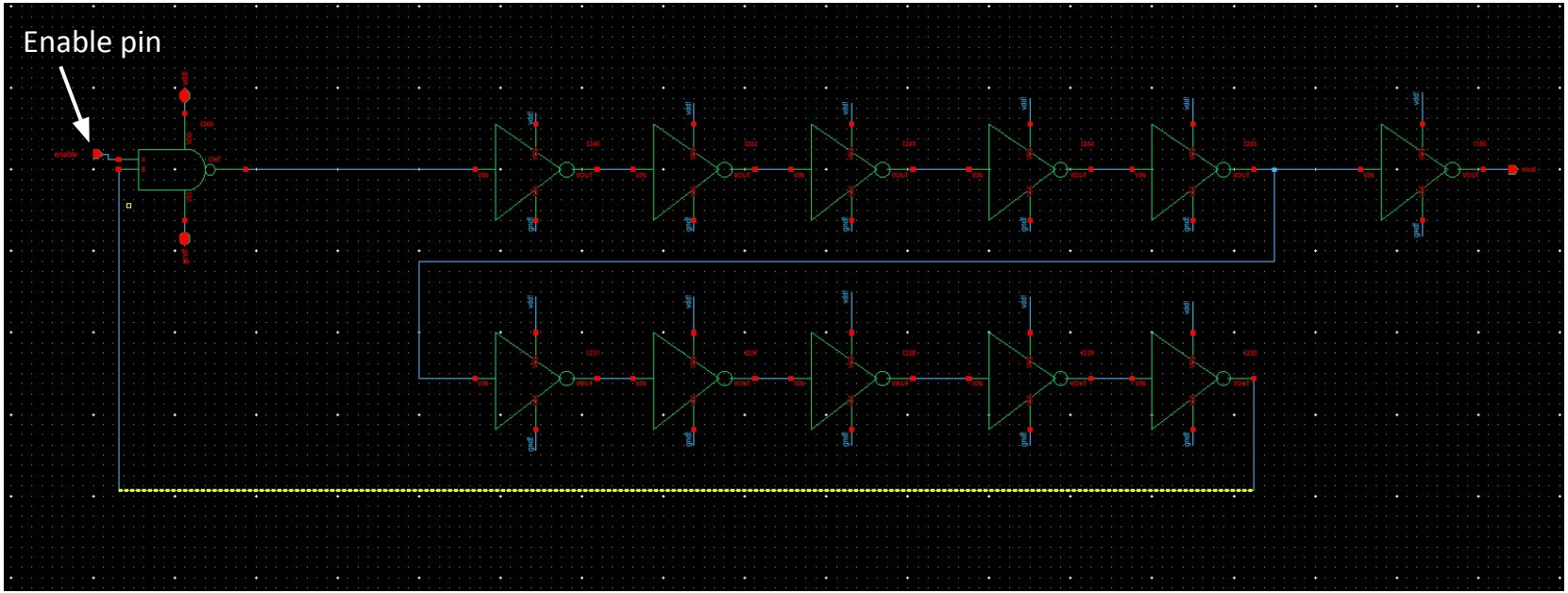
Schematic



Layout

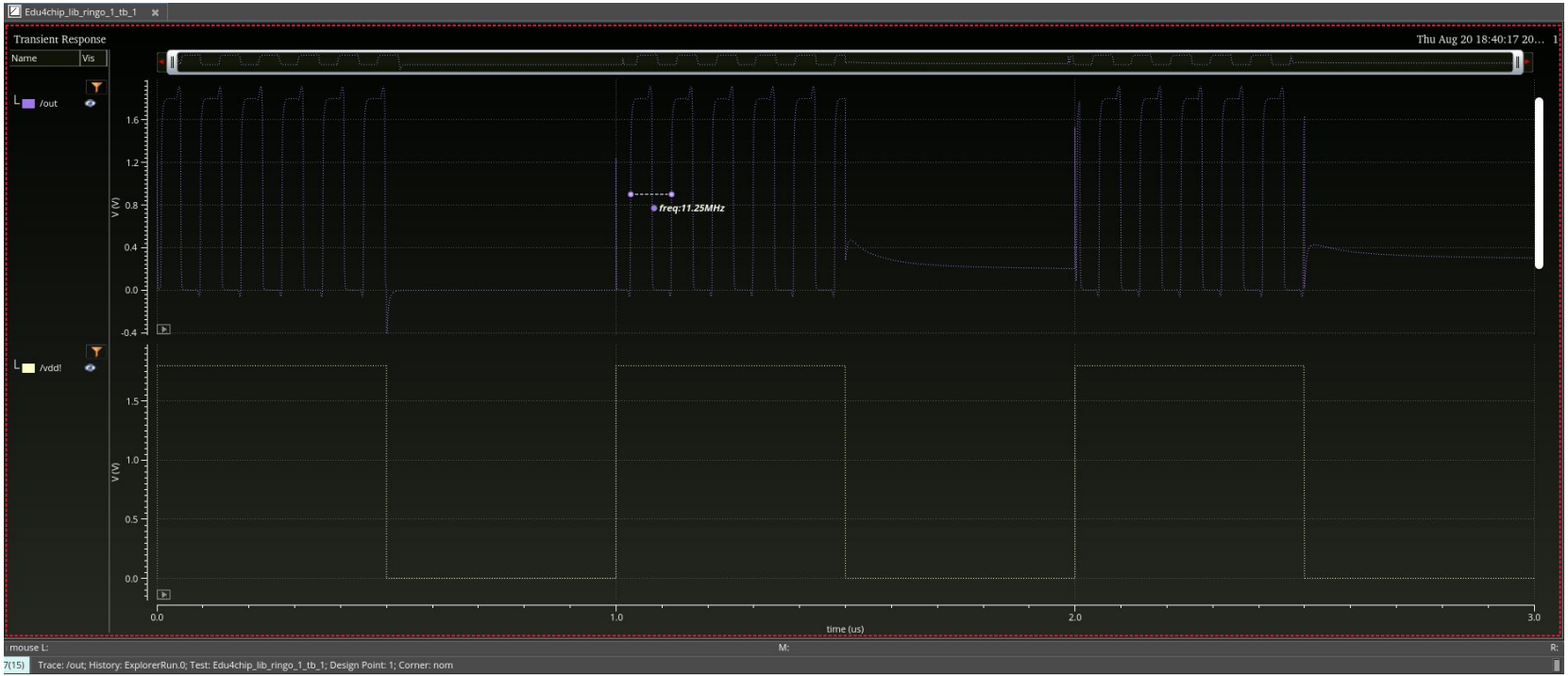


Ring oscillator schematic



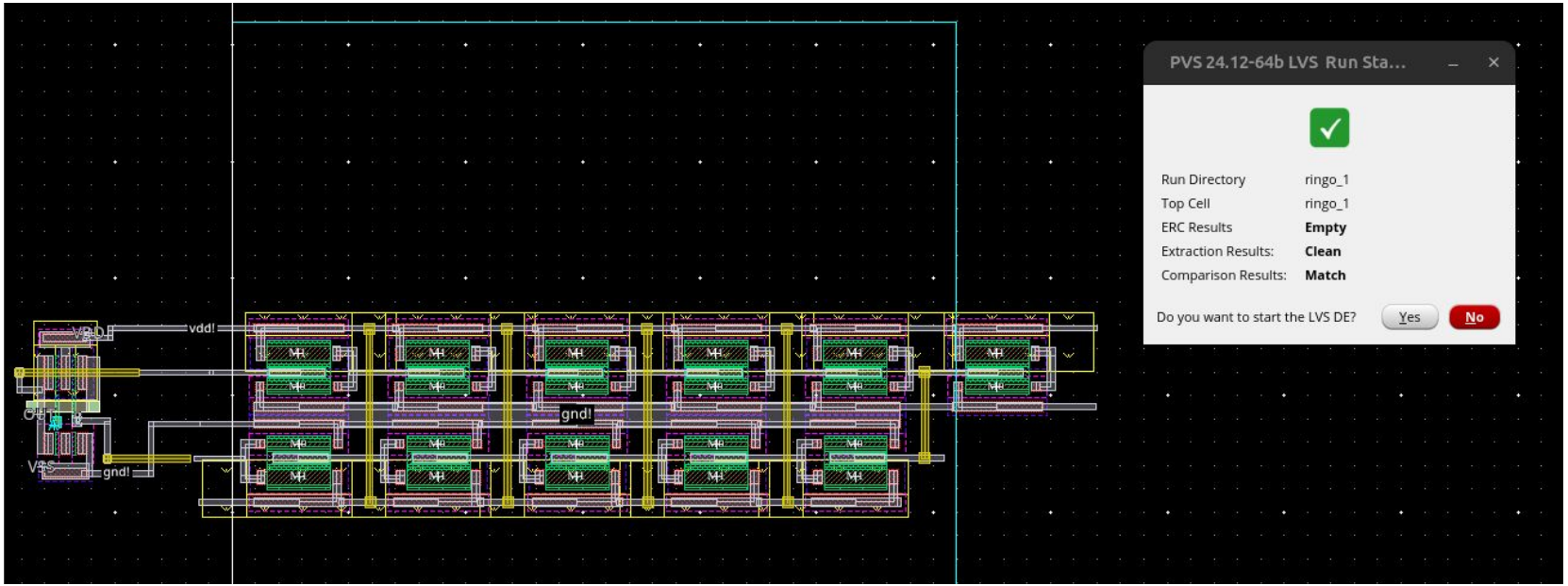
Ringo schematic

Ring oscillator schematic



Pre-layout simulation

Ring oscillator layout



Configuration in two rows (bottom row with mirrored cell for shorter wires)

Method

- Create a model for determining the length of the inverters depending on the amount of inverters
- To simulate the optimal length we ran a sweep with a dynamic variable
- Standardizing the inverter for easy duplication
- Utilizing DRC (Design Rules Check) for layout testing
- Using LVS (Layout versus Schematic) to test the layout plausibility.

Evaluation

Success

- We have achieved the targeted frequency range
- A reasonable amount of gates was used to limit the size
- Included an enable signal through the NAND

Possible improvements

- Calculate the trade-off between multiple inverters vs changing the inverter itself
- Match the rise and fall time of the NAND
- Match the propagation delay of the NAND with the inverter

